REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

After entry of the foregoing amendment, Claims 1, 4-6, 8, 9 and 13 and 15-20 are pending in the present application. Claim 1 has been amended to include the subject matter of canceled Claims 2 and 3. Claim 9 has been amended to include the subject matter of canceled Claims 10 and 12 and Claim 13 has been amended to include the subject matter of Claims 9 and 10. Claims 2, 3, 7 and 10-12 and 14 have been canceled without prejudice or disclaimer. New Claims 15-20 have been added. Support for new Claims 15-20 can be found at least on page 4, lines 28-31 of the specification. No new matter has been added by the above amendment.

By way of summary, the Official Action presents the following issues: The title of the Invention is objected to; the Abstract of the Disclosure is objected to; the drawings are objected to; the specification has been objected to; the claims have been objected to; Claims 1-4, 7 and 9-14 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite; Claims 9-10 stand rejected under 35 U.S.C. § 102 as lacking novelty with respect to Lee et al (U.S. Patent No. 5,890,192, hereinafter Lee), Claims 1-4 and 5-7 stand rejected under 35 U.S.C. § 103 as being obvious over Lee in view of Sukegawa et al (U.S. Patent No. 5,812,814; and Claim 8 stands rejected under 35 U.S.C. § 103 as being obvious over Lee and Sukegawa in further view of Bruce et al (U.S. Patent No. 5,822,261, hereinafter Bruce).

Applicant notes that as the subject matter of Claims 9 and 10 have been incorporated into amended Claims 9 and 13, which include additional limitations, the rejection under 35 U.S.C. § 102 has been rendered moot.

OBJECTION TO THE TITLE

In regard to the objection to the title outlined in paragraph 2 of the Official Action, Applicant has deleted the title in its entirety and substituted a new Title therefor which is clearly indicative of the invention to which the claims are directed.

Accordingly, Applicant respectfully requests that the objection to the title be withdrawn.

OBJECTION TO THE ABSTRACT

In regard to the objection to the Abstract outlined in paragraph 3 of the Official Action, Applicant has amended the Abstract pursuant to the suggestions in the Official Action.

Accordingly, Applicant respectfully requests that the objection to the Abstract be withdrawn.

OBJECTION TO THE DRAWINGS

In regard to the objection to the drawings outlined in paragraph 4 of the Official Action, Applicant submits herewith replacement sheets incorporating the changes suggested in the Official Action. Further, Applicant notes that in Figs. 5-6 address/data/command bus (3) should not be shown as connected to input to the memory device as such data is input sequentially via one line as shown in Fig. 8.

Accordingly, Applicant respectfully requests that the objection to the drawings be withdrawn.

OBJECTION TO THE SPECIFICATION

In regard to the objections to the specification outlines in paragraph 6 of the Official Action, Applicant has amended the specification pursuant to the suggestions outlined in the Official Action. Further, the Applicant has reviewed the specification to ensure that similar errors have been located and corrected.

Accordingly, Applicant respectfully requests that the objection to the specification be withdrawn.

OBJECTION TO THE CLAIMS

In regard to the objection to the claims outlined in paragraph 6 of the Official Action, Applicant has amended the claims pursuant to the suggestions outlined in the Official Action.

Accordingly, Applicant respectfully requests that the objection to the claims be withdrawn.

REJECTION UNDER 35 U.S.C. § 112

In regard to the rejection of Claims 1-4, 7 and 9-14 under 35 U.S.C. § 112, second paragraph as outlined in paragraph 7 of the Official Action, Applicant has amended the claims to correct the cosmetic matters of form and language inconsistencies identified in the Official Action.

Accordingly, Applicant respectfully requests that the rejection of Claims 1-4, 7 and 9-14[1] under 35 U.S.C. § 112, second paragraph be withdrawn.

[1] Language of the canceled claims has been amended in incorporated form in the pending claims.

REJECTION UNDER 35 U.S.C. § 103

The Official Action has rejected Claims 1 and 4-6 under 35 U.S.C. § 103 as being unpatentable over Lee in view of Sukegawa. The Official Action states that Sukegawa discloses all of the Applicant's claim limitations with the exception of a plurality of memory circuits provided on a memory chip. The Official Action cites Lee as disclosing this more detailed aspect of the Applicant's invention and states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references to arrive at the Applicant's claims. Applicant respectfully traverses the rejection.

Amended Claim 1 recites, *inter alia*, an electrically rewritable nonvolatile semiconductor memory device including:

> ". . . a master chip enable terminal for controlling the activity and inactivity of said memory chip as a whole, the activity and inactivity of each of said memory circuits being controlled by a logical output of a signal of said master chip enable terminal;
> wherein each of said memory circuits is provided with a ready/busy signal terminal which corresponds to a respective chip enable terminal."

By way of background, electrically erasable programmable read-only memory (EEPROM) are utilized in conjunction with control circuitry of the EEPROM for writing/erasing data therefrom. During this writing/erasing process, further operations are delayed until the writing operation is completed. Thus, if an attempt is made to write further data to the EEPROM during a write cycle, a busy signal will inhibit access to the EEPROM. Thus, in order to realize a high-speed performance in such a memory system, a time sharing control technique employing a parallel processing configuration is desired.[2]

[2] Application at pages 1-2.

In light of the above deficiency in the art, the present invention is provided. With this object in mind, a brief comparison of the claimed invention in view of the cited references is believed to be in order.

Sukegawa discloses a semiconductor memory system (100) including a plurality of EEPROM chips (101-106). The EEPROM chips include a cell array and a plurality of peripheral logic functions, such as a row address decoder, for the cell array. Each EEPROM chip has an input/output register, and the chips are accessed by providing an initial memory address of a unit amount of data.[3] The EEPROM chips are connected to a controller unit (130) via a common I/O bus and a common read/write control (R/W). Each EEPROM chip is independently connected to the control unit via a chip select signal and a ready/busy signal line.[4]

In operation, after address conversion, an access controller (132) selects one of the EEPROM chips (by providing a signal to one of the chip-select signal lines CS1-CS6) and generates a real memory address. The access controller manages the rewrite (or erasing) of each erasable block in each EEPROM chip for a number of times equal to the rewrite count information in each EEPROM chip. Thus, the access controller provides a chip enable signal (CE) to indicate an active state for the EEPROM chip selected by the address conversion. Next, the access controller provides a memory command for indicating an operation mode (write, read, erase, verify and so on) to the EEPROM chip via a read/write control line.[5]

Lee discloses a memory system for improving access speed. As shown in Fig. 2, multiple data (chunks) are written concurrently into a EEPROM device. A chunk address and data information for each of the multiple data chunks is first provided to corresponding latches in the EEPROM device. Next, a program command ordering write circuitry in the

[3] Sukegawa at column 4, lines 6-20.
[4] Sukegawa Fig. 2.
[5] Sukegawa at column 6, lines 13-18.

EEPROM device to concurrently write the provided chunks of data into the locations indicated by the chunk addresses, which in turn, is followed by a signal wait period for the multiple data chunks to be concurrently programmed and verified before writing a next multiple data chunks into the EEPROM device. In this way, as only a signal program/verify wait period is incurred in this multi-chunk write operation, it is performed considerably faster than prior art designs.[6] Lee discloses that subarrays of the memory are selected by addresses (AXL and AYL), not a master chip enable signal (MCE).

Conversely, Applicant's invention is directed to a high-speed processing memory system. The system provides an electrically erasable programmable read-only memory device capable of controlling a signal memory chip similar to a plurality of memory chips. To this end, a master chip enable (MCE) function is employed for controlling the activity and inactivity of the memory chip as a whole and the activity and inactivity of each of a plurality of memory circuits is controlled by a logical output of a signal of the master chip enable terminal. As neither Sukegawa, alone or in combination with Lee, disclose the Applicant's invention as presently recited in amended Claim 1, Applicant respectfully requests that the rejection of Claim 1 under 35 U.S.C. § 103 be withdrawn.

Claims 4-6 recite substantially the same limitation discussed above by virtue of dependency and/or independent recitation. Therefore, Applicant respectfully requests that the rejection of Claims 1, and 4-6 under 35 U.S.C. § 103 be withdrawn.

The Official Action has rejected Claim 8 under 35 U.S.C. § 103 as being unpatentable over Sukegawa and Lee in view of Bruce. The Official Action states that Sukegawa and Lee disclose all of the Applicant's claim limitations as discussed above with the exception of providing a common ready-busy signal terminal. The Official Action cites Bruce as disclosing this more detailed aspect of the Applicant's invention and states that it

[6] Lee at column 3, lines 15-31.

would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the references for arriving at the Applicant's claim. Applicant respectfully traverses the rejection.

As discussed above, neither Sukegawa not Lee disclose or suggest Applicant's memory system which includes a master chip enable for controlling the activity and inactivity of the memory chip, and the activity and the inactivity of each of a plurality of memory circuits being controlled by a logical output of a signal of the master chip enable terminal. Thus, none of the cited references, either alone or in combination, can be properly asserted as disclosing or suggesting Applicant's Claim 8, which includes the above distinguished limitations by virtue of its dependency. Therefore, the Official Action does not provide a *prima facie* case of obviousness with regard to Claim 8.

Accordingly, Applicant respectfully requests that the rejection of Claim 8 under 35 U.S.C. § 103 be withdrawn.

NEW CLAIMS

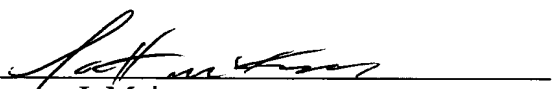
New Claims 15-20 have been added to recite a further aspect of the Applicant's invention. In addition to the reasons discussed above, none of the cited references disclose or suggest a stacked gate structure including a NAND configuration. Accordingly, Applicant respectfully submits that new Claims 15-20 are allowable over the references of record.

CONCLUSION

Consequently, in view of the foregoing amendment and remarks, it is respectfully submitted that the present application, including Claim 1, 4-6, 8, 9, 13 and 15-20 is adequately described, patentably distinguished over the prior art, in condition for allowance, and such action is respectfully requested at an early date.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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